

After Sales Technical Documentation

RAE/RAK-1N Series

Chapter 8

Faultfinding/Disassembly

CONTENTS –Faultfinding

	Page No
General	8 – 3
Disassembly Procedure	8 – 4
LCD / UI Module Disassembly(see fig.1)	8 – 4
System Module Disassembly (see fig.2)	8 – 6
PDA Faultfinding	8 – 8
Introduction	8 – 8
Required Servicing Equipment:	8 – 8
Block Diagram	8 – 8
PDA Components	8 – 9
PDA Troubleshooting Diagram	8 – 10
1 Troubleshooting Diagram of the Power-On Malfunction	8 – 12
2 Troubleshooting Diagram of the POST-Code	8 – 23
3 Troubleshooting Diagram of the LCD Check	8 – 24
4 Troubleshooting Diagram of the Buzzer	8 – 29
5 Troubleshooting Diagram of the PMI Check	8 – 31
6 Troubleshooting Diagram of the Keyboard	8 – 34
7 Troubleshooting Diagram of the InfraRed Check	8 – 37
8 Troubleshooting Diagram of the RS-232 Check	8 – 40
Appendix A	8 – 42
Appendix B	8 – 43

Figures

Figure 1. LCD / UI Module disassembly	8 – 5
Figure 2. System Module disassembly	8 – 7

General

The purpose of this document is to provide methods of finding component malfunctions in the PDA module of the Communicator.

Note:—Due to the large integration scale used it is not always possible to pinpoint the faulty component. However the flow diagrams introduced here should act as a useful guide for these purposes.

Required servicing equipment:

- PC for the service software
- power supply
- RS cable
- digital multimeter
- oscilloscope
- frequency counter (optional)

Disassembly Procedure

LCD / UI Module Disassembly (see fig.1)

1. Remove 4 stick-on screw caps (A) and 4 Torx screws (B).
2. Gently remove the module sub-assy by pushing the keypad down.
Note: The right lower screw tower is the most difficult one to release.
3. Disconnect flexi connectors (D) then (C) by releasing connector clips. Connector C will open by lifting the clip up.
4. Unplug the coaxial antenna wire. (E).
5. Remove EMC flex (not shown) from the reverse side of the UI module card and then remove the module assembly. (F).
6. Remove PDA LCD module assy. (H)
7. Unclip screen frame (G) from the LCD module.
Note: LCD module is attached to the frame by double sided tape.
8. Re-assemble in reverse order ensuring the following:
 - correct orientation of PCB in frame, i.e. connector D should be in line with the scroll keymat.
 - Coaxial antenna cable (E) does not go under the UI module or it will disable the function keys.

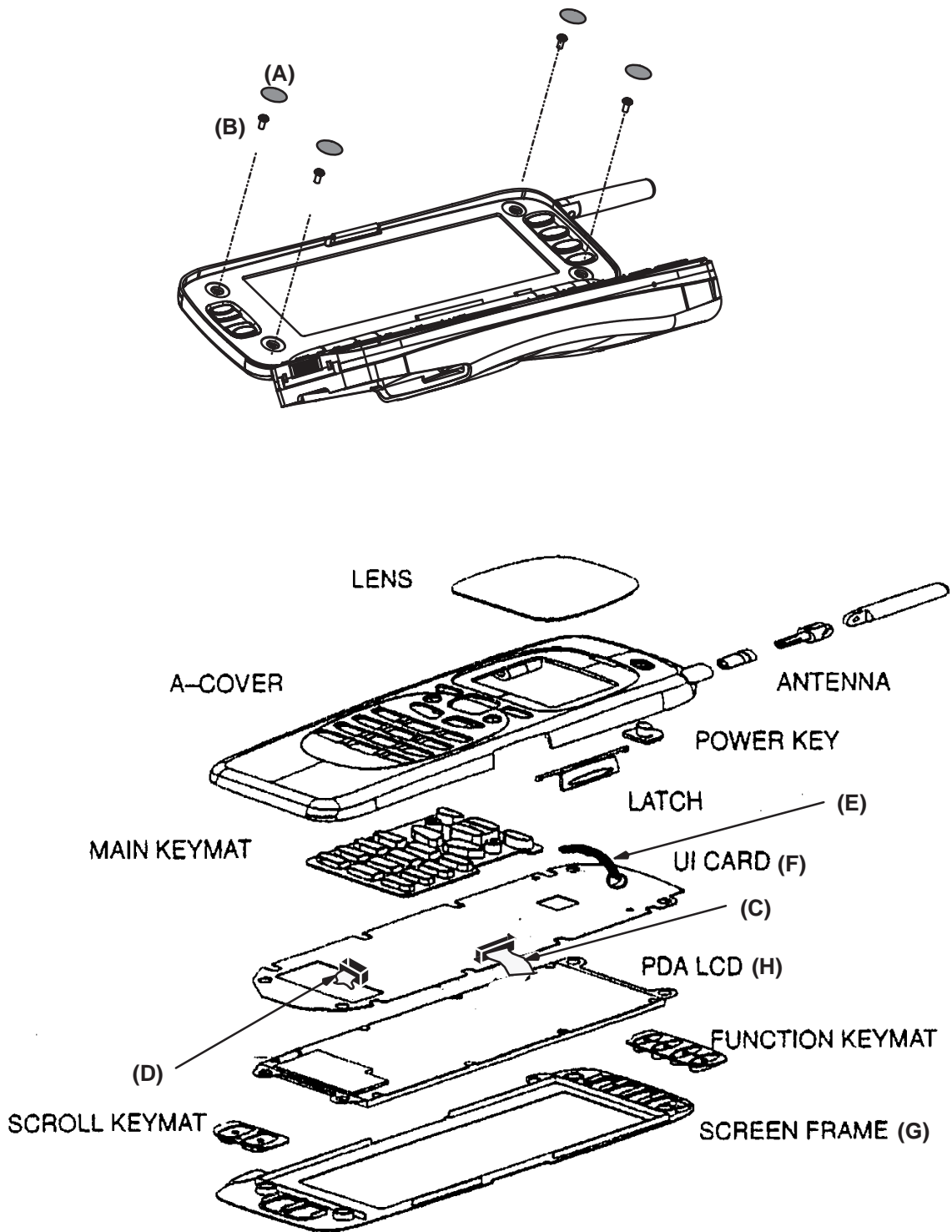


Figure 1. LCD / UI Module disassembly

System Module Disassembly (see fig.2)

1. Remove Battery. (A)
2. Remove 2 Torx screws. (B)
3. Gently lift off C cover (C) starting from the battery hole.
Note: be aware that the speaker gasket on the SIM-flex might stick to the C cover buzzer gasket.
4. Remove 7 torx screws, (D) do not undo screws marked with an S on the diagram yet.
5. Remove coaxial antenna cable. (E)
6. Remove EMC flex (not shown) from the top of the shield.
7. Lift out the sub-assy.
8. Remove PDA module card (I) from the chassis by lifting it in the middle.
9. Remove the handsfree speaker from the chassis.
10. Open the SIM-flex connector on the CMT module and unplug the SIM-flex from the chassis. (F)
11. Remove 3 short Torx screws (S), open the shields and remove the CMT module.
12. Re-assemble in reverse order and observe the following points:
 - Ensure the shield snaps into position properly.
 - Position the handsfree speaker gasket so that the sound gap in the chassis is open and the speaker wires are not trapped between the PDA module and chassis.
 - Check that the handsfree microphone wires go through the slot in the chassis and do not get trapped between the chassis and PDA module.
 - Position the EMC flex with guide lines on the shield.
 - When re-assembling the sub-assy and cover, locate the system connector end of the assy first.
 - Ensure the handsfree microphone dust washer inside the cover remains in place.
 - Position the coaxial antenna cable so that it goes around the screw tower. The black mark on the cable is the correct fixing point for the cover.

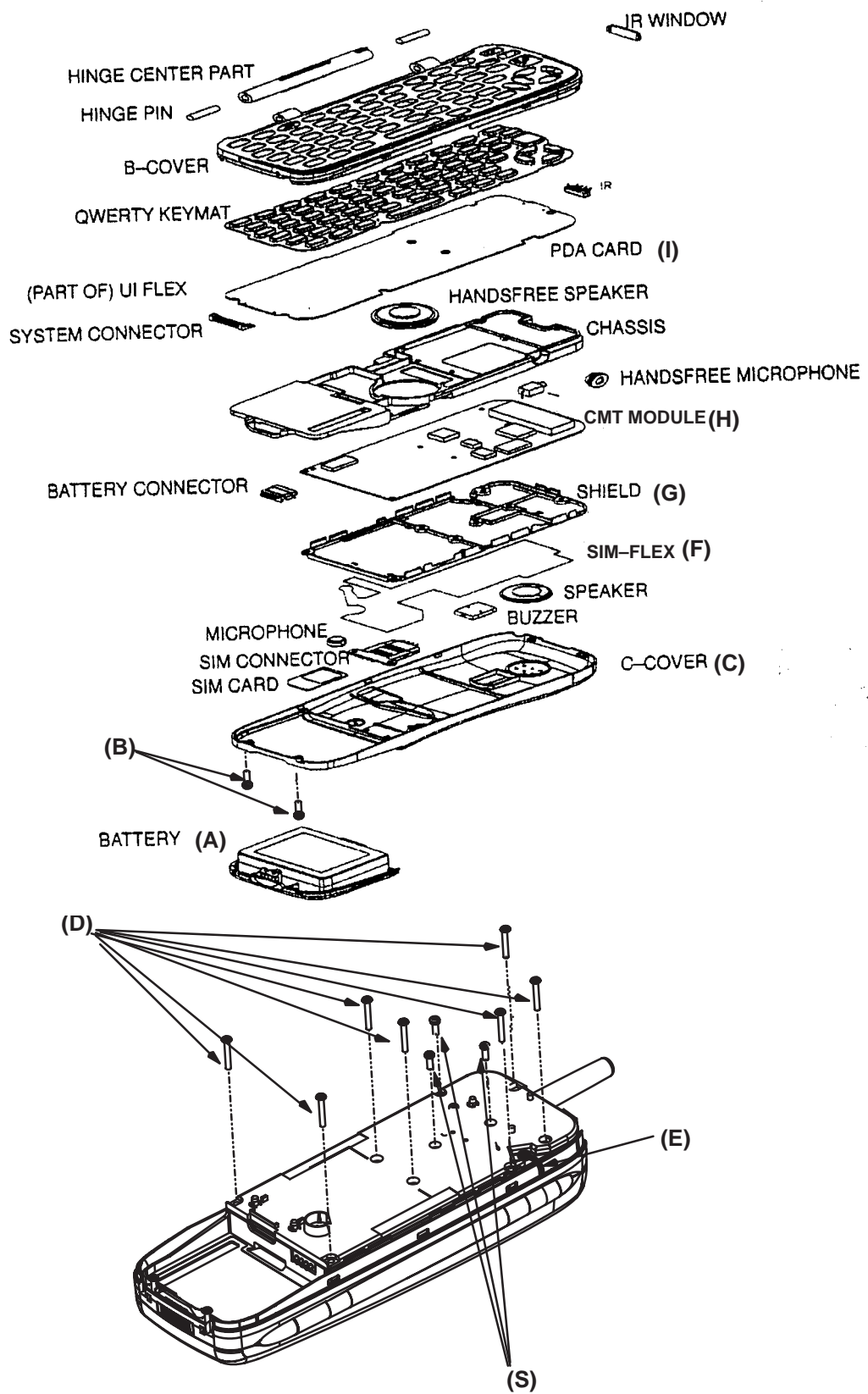


Figure 2. System Module disassembly

PDA Faultfinding

Introduction

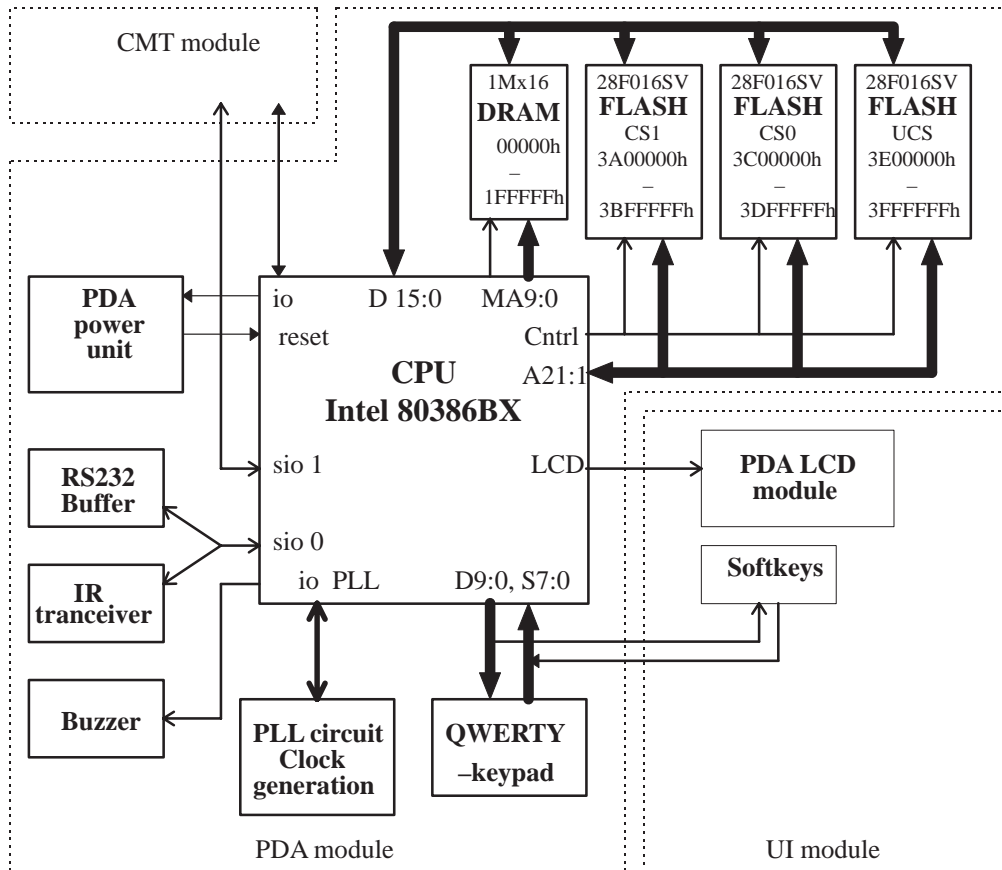
The purpose of this document is to provide methods to find the component that is malfunctioning in the PDA module of the Communicator. Due to the large integration scale used in the Communicator, it is always not possible to point the faulty component for sure. However the flow diagram introduced here is made to fulfill the aim as well as it is possible.

Required Servicing Equipment:

- PC for the PCLocals
- power supply
- RS cable
- digital multimeter
- oscilloscope
- frequency counter (optional)

Block Diagram

The block diagram of the Communicator PDA is described in the picture below:



PDA Components

The following components of the Communicator PDA have an dramatic effect to the functionality of the module, a fault in any of these may cause the module to appear totally 'dead':

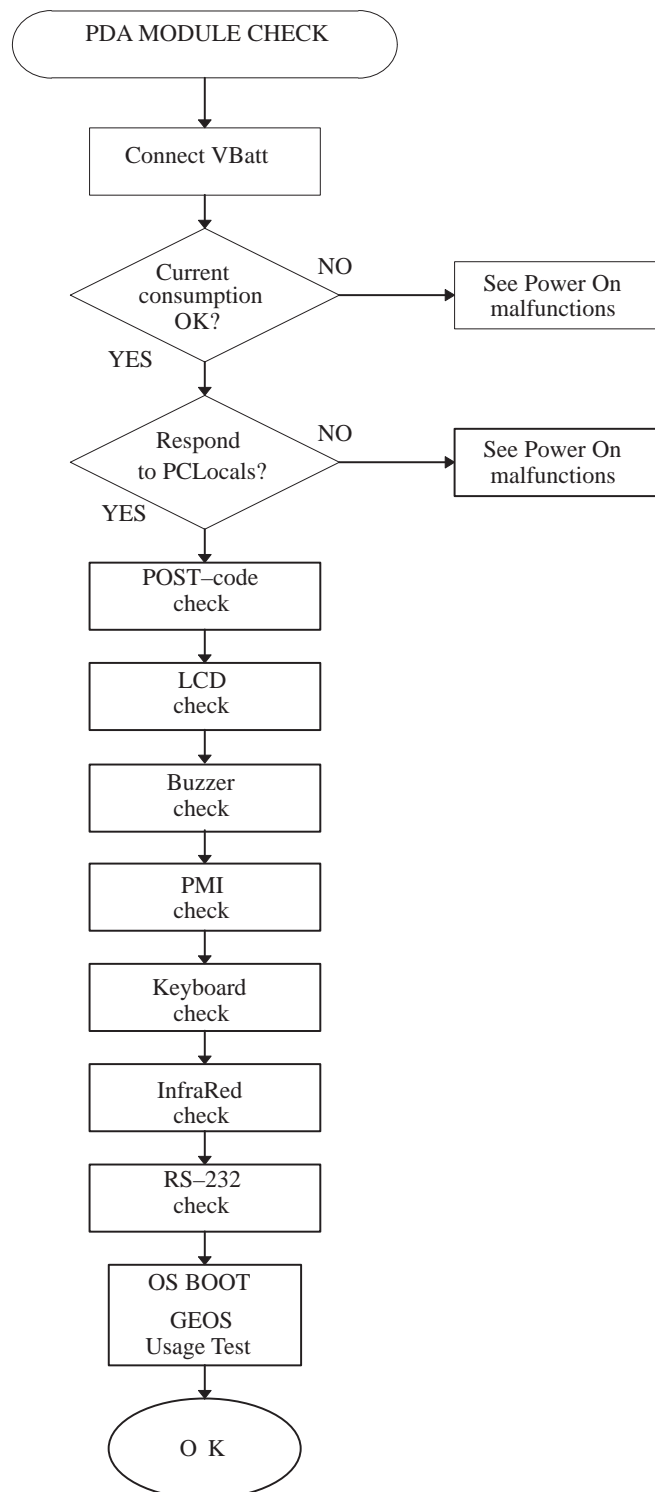
- PDA power unit
- CPU
- PLL clock generation circuit
- UCS Flash chip

If the device has some functionality, then the following components, along with the ones above, can be tested:

- DRAM chip
- CS1 and CS0 Flash chips
- RS buffer
- buzzer
- IR tranceiver
- keyboard
- LCD module

PDA Troubleshooting Diagram

The highest level of PDA troubleshooting is shown in the following flow chart. All diagrams assume that the unit has been checked for short circuits and loose pins.



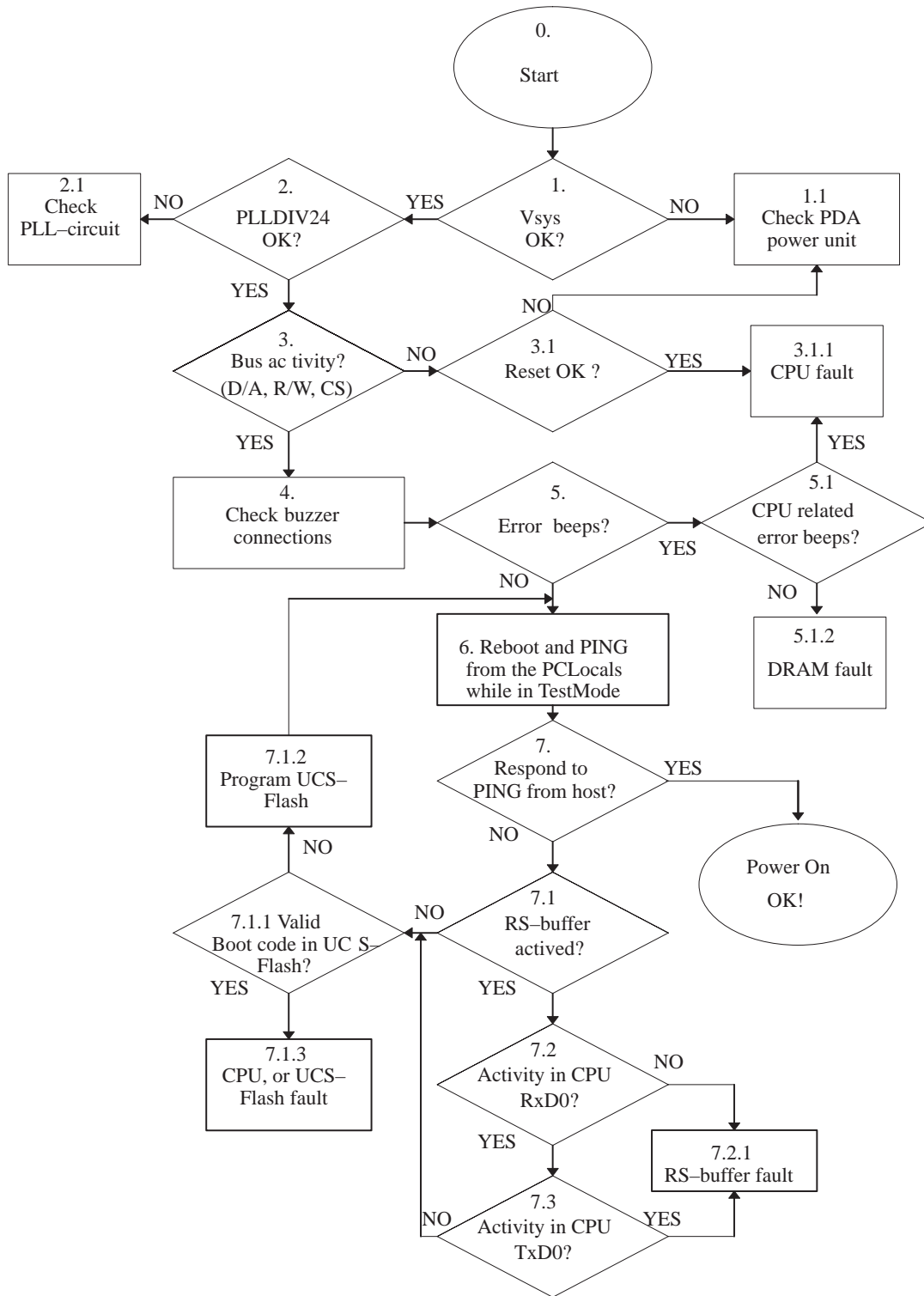
The module check begins with connecting the supply voltage to the PDA. If the current consumption differs a great deal from the normal limits, proceed to the Power-On check.

If current consumption is OK, the service software should connect to the PDA. If the target PDA does not respond to the pings from the host, check the Power-On procedure.

When the PDA responds further tests may be carried out; the execution order is not significant and it may be changed.

After all the functional tests are working, the device under test should be re-booted, and the normal usability of the GEOS, along with the CMT module should be checked before the PDA can be considered to be fully functional.

1 Troubleshooting Diagram of the Power-On Malfunction



1.1 Vsys OK?

Start the Power-On check by connecting the power supply to the target. The power supply voltage limits are: 5.8V (min.) – 7.2V (nom.) – 8.5V (max), The current consumption in a working PDA is typically about 120mA.

If the Vsys is out of the limits (2.97V..3.66V) or the current consumption differs from the normal, then check the PDA power unit.

1.1.1 Check PDA Power Unit

The following picture illustrates the troubleshooting diagram that can be used with the PDA power unit malfunctions. As a rough check it is good to glance through the power section of PDA module and check that there are no short circuits by alien particles and that no component has 'burning' signs, especially tantalum capacitors. If yes, the fault is most probably cured by replacing that component. In such a case it is recommended that the complete power unit check is done after replacing the faulty component.

If power unit check is not solving the problem there is a possibility that battery line or some regulator output has a short circuit somewhere. Vsys is distributed all over the board and it may be difficult to find possible short circuit cause. There are test strips going to the edge of PCB in middle layers. The strips are cut when the module is cut from the panel in production. If the device is used in high moisture environment it is possible that those copper strip ends corrode and form some ohmic short circuit to neighbouring strips. Use of glass fibre brush to test strip 'necks' on the edge of PCB is recommended. Current supplying capabilities of different regulators are: Vsys:500mA, VCC5:50mA, LCDVEE:5mA. Each current is for the specific regulator output voltage. VCC5 is linear regulator, VSYS and LCDVEE are made by switch mode regulators.

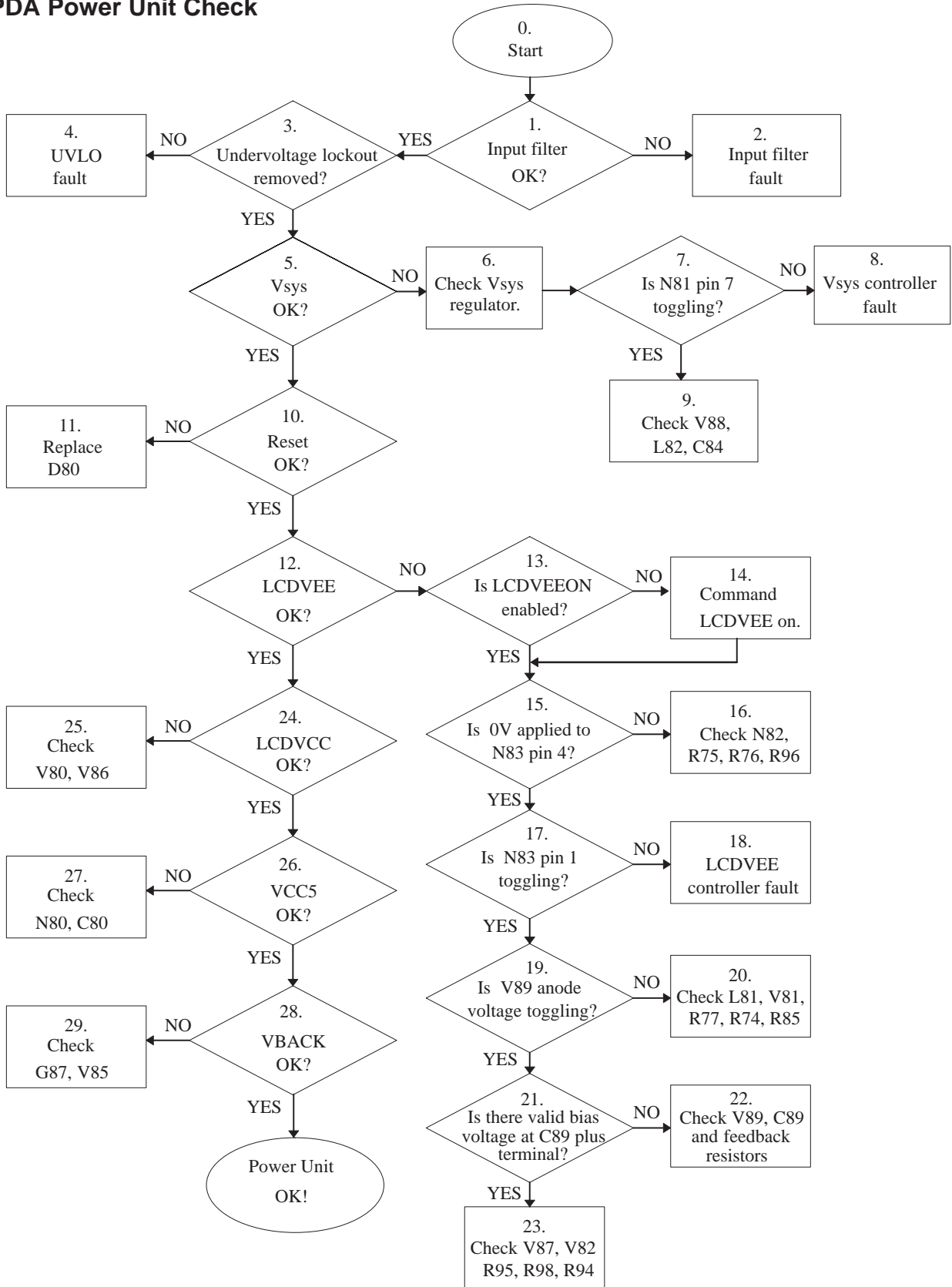
1.1.1.1. Input filter OK?

Between board-to-board connector battery line and regulators there is LC-filter to reduce interference conducting through battery line from CMT to PDA module and visa versa. Overcurrent and overvoltage may damage filter components. If battery voltage is not seen in equal value at positive terminal of C83 and at board-to-board connector battery line then check that L80 is not open circuited. If not check that C81 and C83 are not short circuited to a finite resistance (<100 ohm) and there is no visible damage in capacitors. If fault is still not found check also bypass capacitors C93, C94, C96, C87 and C97.

1.1.1.2 Input filter fault

Replace faulty component. If fault is not focused try to change tantalum capacitors first. If that is not helping there is a possibility that one of the IC's N80, N81, N82 or N83 has internal short circuit.

PDA Power Unit Check



1.1.1.3 Undervoltage lockout removed?

This UVLO is made as hardware limit to shut down V_{sys} if battery voltage drops below 5.0V. **When the N82 comparator controlling N81 has worked the shutdown of V_{sys} is cancelled only after battery voltage rises over 6.0V!** It is possible to test PDA module at voltages between 5.0V and 6.0V but wakeup of V_{sys} requires voltage higher than 6.0V. This hysteresis is put to design to prevent oscillation at low battery voltages after battery cutoff limit is reached and battery voltage rises after its load is removed.

If battery voltage is higher than 6.0V, battery voltage (nearly) should be seen at regulator N81 pin 1. If not go to 1.1.1.4.

1.1.1.4 UVLO fault

First check that 4.1V can be measured from reference V84 cathode. If not replace V84 and check R88. Next check that voltage between R87 and R89 is higher than voltage across V84. This voltage should be reduced to V84 voltage level if battery voltage is reduces to 5.0V. If not check R87, R89 and R65.

If above mentioned is OK check R80. If OK replace N82.

1.1.1.5 V_{sys} OK?

Measure V_{sys} voltage for example from C84 positive terminal. It should be between 3.135V and 3.465V. If not go to 1.1.1.6.

1.1.1.6 Check V_{sys} regulator

First check that battery voltage is seen at N81 pins 3 and 8. If pin 3 is low regulator does not exit from 'soft start' state.

1.1.1.7 Is N81 pin 7 toggling?

If measured with oscilloscope there should be seen voltage level toggling between 0V and V_{Batt} at frequency of about 200kHz. If not go to 1.1.1.8. Otherwise go to 1.1.1.9. If the regulator has dropped to a shutdown state the pulse frequency is lower and pulses appear at irregular time intervals.

1.1.1.8 V_{sys} controller fault

Replace N81.

1.1.1.9 Check V88, L82, C84

If the controller N81 tries to alternate pin 7 level, even at reduced voltage magnitude the fault is very likely found from V88, L82 or C84. If the problem is still unsolved check that V_{sys} current consumption is less than 500mA. Reasonable value is about 200mA when CPU is fully on. If not there must be a short circuit in V_{sys} line.

1.1.1.10 Reset OK?

The PWRGOOD signal should go from low to high after minimum time of 140ms when Vsys has risen to a valid level. Time between battery connection and valid voltage at Vsys line should be in the order of 1.5ms. If PWRGOOD signal rises too fast, or the signal levels are illegal, then go to 1.1.1.11.

1.1.1.11 Replace D80

If this is not helping PWRGOOD line is pulled up or down somewhere or there is a CPU fault.

1.1.1.12 LCDVEE OK?

In boot sequence LCD is on. If voltage other than 20V – 24V near room temperature is seen at LCDVEE terminal then go to 1.1.1.13.

1.1.1.13 Is LCDVEEON enabled?

There is LCD bias voltage shutdown feature in PDA normal use after set inactivity time period. Check that LCDVEEON line is in logic high state (3.0V – 3.4V). If not go to 3.1.1.14. Otherwise go to 1.1.1.15.

1.1.1.14 Command LCDVEE on

Use PC Locals to command LCDVEE permanently on. Select 'I/O–Space Functions'/'Target Signal Control' to toggle LCDVEE. This menu can also be used to control LCDVCC, flash program voltage (VCC5) and LCDPWM. When LCD module is not connected verify also LCDVEE off state by toggling the control by PCLocals.

1.1.1.15 Is 0V applied to N83 pin 4?

Check that voltage between 0V and 0.3V is seen at N83 controller pin 4. This signal enables the controller. If not go to 1.1.1.16. When LCD module is not connected verify also LCDVEE off state by toggling the control by PCLocals. In LCDVEE off state N83 pin 4 must see battery voltage.

1.1.1.16 Check N82, R75, R76, R96

First check that resistors R75, R76 and R96 are OK. Check that voltage at comparator N82 pin 3 is in the range of 1.55V – 1.75V. If not check reference V84. In cathode of V84 voltage of 4.1V should be seen. If OK replace N82. After that if still problems verify that comparator N82 pin 2 has higher voltage than pin 3. If yes and N82 pin 1 is not low (0V – 0.3V) then change N83.

1.1.1.17 Is N83 pin 1 toggling?

There should be seen about 300kHz voltage toggling between 0V and VBatt. In oscilloscope there should be seen about 20 pulse sequences at irregular pulse group periods. If not go to 1.1.1.18. Otherwise if there are pulses coming to N83 pin 1 in continuous train the regulator is 'saturated'. Check that valid LCD voltage is seen at C89 positive terminal. Measure LCDV_{EE} current with UI module connected. If current is higher than 4mA big LCD in UI module is probably corrupted.

1.1.1.18 LCDV_{EE} controller fault

Replace N83.

1.1.1.19 Is V89 anode voltage toggling?

There should be seen irregular shaped voltage bursts at peak magnitude between 0V and valid LCD voltage (little higher). Voltage bursts decrease in magnitude during their period. The bursts appear at irregular time intervals. If not go to 1.1.1.20.

1.1.1.20 Check L81, V81, R77, R74, R85

Most probably V81 is broken. Check and replace. If not helping check L81 and R74, R85. These resistors provide current feedback information to the controller. There should be seen increasing voltage spikes at peak magnitude of a little less than 300mV. If yes L81, V81, R74 and R85 are OK. Then check and replace V89.

1.1.1.21 Is there valid bias voltage at C89 plus terminal?

Measure DC voltage over C89. It should be within 20V – 24V at room temperature. Measure also peak-to-peak AC voltage from 100ms sample. It should be less than 100mV. If not go to 1.1.1.22. If yes go to 1.1.1.23.

1.1.1.22 Check V89, C89 and feedback resistors

First measure voltage from N83 pin 3. It should be exactly 1.5V. If yes replace C89. Also check C95 and V89. If not check resistance and replace if needed for resistors: R84, R82, R78, R93 and R97. Also check C79.

1.1.1.23 Check V87, V82, R95, R98, R94

The fault is that the regulator works correctly but the switch between the regulator and LCD module is broken. This switch is needed to totally cut voltage from LCDV_{EE} line. First measure collector voltage of V87. It should be near 0V. If not check and replace V87, R95 and R98. If yes replace V82. Also check R94 and R98.

1.1.1.24 LCDVCC OK?

Command LCDVCC on by PCLocals. Measure voltage from LCDVCC line. If the voltage differs from Vsys value go to 1.1.1.25. When LCD module is not connected verify also LCDVCC off state by toggling the control by PCLocals.

1.1.1.25 Check V80, V86

Transistor V80 gate is pulled down by transistor V86 to enable LCDVCC. Identify and replace the faulty transistor. If not helping then check also R81, R72 and C91.

1.1.1.26 VCC5 OK?

Command VCC5 on by PCLocals. Measure voltage from VCC5 line. If the voltage is other than 5.00V \pm 50mV go to 1.1.1.27. The delay between regulator enable and valid voltage at output should be less than 0.1ms.

1.1.1.27 Check N80, C80

Check that CPU enable signal comes to regulator pin 3. If yes try to disconnect VCC5 load by bending up N80 pin 5 and attaching output capacitor to the pin. If regulator works after that there is failed ohmic connection in VCC5 line or in FLASH memories. Otherwise check and replace N80, C80.

1.1.1.28 VBACK OK?

Measure backup battery voltage from battery terminals. If that is less than 2.8V backup battery is about to be empty in near future (80% used). Then it is reasonable to change the battery in order to save customer from inconvenience in near future. In order to do complete test disconnect main battery from the module. If voltage in VBACK line is under 2.6V go to 1.1.1.29.

With PC Locals it is possible to check whether the VBACK voltage has been on illegal level before boot. This can be checked only once after each boot, and then after the VBACK is considered to be OK.

1.1.1.29 Check G87, V85

Check that voltage over G87 is 2.8V or higher. If not check that there is maximum 35mV drop over resistor R90. If the drop is higher, RTC circuitry in VBACK line take too much current. If the drop is OK check that VBACK line voltage drop in diode V85 is less than 150mV. If not replace V85.

1.2 PLLDIV24

If the V_{sys} and the current consumption is OK, check whether the PLL circuitry and the clock generation inside the CPU (D130) is working properly. The output of pin 110 of the CPU should be a square wave and the frequency in A5 stepping of the CPU 307kHz, in the A3 stepping of the CPU the frequency should be 614kHz. The shape and the frequency can be checked with a scope, the frequency can be measured more accurately with a frequency counter.

If the frequency is OK, then proceed to 1.3 otherwise check the PLL circuitry 1.2.1

1.2.1 Check PLL Circuitry

The crystal and circuitry around it can be checked by connecting oscilloscope XTALI signal. On that point a 32.6 – 32.8 kHz signal with 2.5 – 3.5V peak to peak AC amplitude should be found. The signal waveform can vary from almost square wave to sine wave. If this signal can not be detected and VCCRTC level is 2 – 3V then check crystal and circuitry (R140, R141, R146, R147, C155, C156) around it. It is also possible that the actual CPU chip is defective.

If the XTALI signal is OK but PLLDIV24 signal is not available, LPLLI components (R136, C151, C152) and IREFL (R138) must be checked V131, C147 and C149 are also crucial for PLL functionality. If all these seem to be OK, the actual CPU chip is probably defective.

1.3 Bus Activity in Address/Data, Read/Write and Chip Selects?

If the PLL is functional, then the CPU system clock should be running and should try to fetch code from the Flash that is controlled by the UCSX.

Analyzing the code fetching cycles is beyond the scope of this document, and is not needed during normal troubleshooting. The main idea of this is just to check the signal levels, and to see that there is something happening, i.e. the CPU is not totally 'dead'.

If there is some bus activity in all data lines and the signal levels are adequate, the data bus can be considered to be functional. If there is some bus activity in the lower address lines and the signal levels are adequate, the address bus can be considered to be functional. The CPU should also try to read data from and to the memories also the UCSX line should toggle within normal voltage limits. If there are illegal signal levels, the faulty component can be isolated by disconnecting each component in the signal line one by one.

The cycles vary according to the code in the D163 Flash and therefore there is not necessarily no activity in MEMWX and the CS1/CS0 lines.

If there is no activity at all, then check PWRGOOD signal during powering the device up. If there is reasonable activity in the signals and the signal levels are OK, proceed to 1.4

1.3.1 Reset OK?

The PWRGOOD signal, coming from the PDA power unit, should go from low to high after 140ms when VBatt is connected. If this signal is not functioning as expected, then disconnect the signal either from the CPU (D130) or the Reset IC (D80), and isolate the problem to the power unit or to the CPU.

If this signal rises too fast, or the signal levels are illegal, then check the power unit. If the signal is OK, but there's no bus activity at all, then suspect a CPU fault, see 1.3.1.1

1.3.1.1 CPU Fault

If the PLL is running properly and the CPU gets the RESET signal from the power unit (PWRGOOD), but there is no bus activity at all, then it is likely that the CPU is not functioning properly.

If the PLL circuitry surrounding the CPU is OK, but the PLLDIV24 is not, then it is likely that the CPU is defective.

It is possible that PLLDIV24 is OK as well as RESET but no activity is detected on CPU address lines. Before you replace the CPU it is reasonable to check that circuitry around the HPLLI (R137, C153, C154) and IREFH (R139) is OK. It is hard to measure these signals so a visual check is usually all that can be done. If no defect can be found, suspect a defective CPU chip.

If the device beeps during POST CPU related error beeps, then it's likely that the CPU is defective.

1.4 Check Buzzer Connections

In the case of POST found error, the PDA can beep an error code. The list of the possibly error codes can be found in the appendix A. In order to hear the possible beeps, the connection from the CPU (D130) pin124 to the buzzer must be functional, i.e. the SIM flex should be connected to the CMT, and the PDA-CMT connection must carry a BUZZEROUT signal.

The beeps can be also seen using a scope connected to the CPU, pin 124, where the beeps generate a square wave. If the signal can be seen but no sound is heard, then check the circuitry R142-R148, V132-V135, C138, and the SIM flex etc.

1.5 Error Beeps

If there are some error beeps, then make the difference between CPU- and DRAM-related errors and proceed to the CPU/DRAM fault. If no beeps are generated then proceed to 1.6

1.5.1.2 DRAM Fault

If DRAM related error beeps can be heard, then check the resistors R180 – R195. If they are OK, then the fault can be either in the CPU (D130) or in the DRAM itself (D160). As the DRAM is easier to change, it is better to try that first.

1.6 Reboot and PING from the PC Locals while in Testmode.

Next try to establish a connection from the service software to the PDA. Activate the testmode pin of the PDA. Select a menu from the software that pings the target, and then reboot the PDA.

Pinging the target sends bytes (55h) to the PDA via the serial RXD, and waits for a response byte (AAh) from it via the TXD.

1.7 Respond to PING from the Target

If the target PDA respond to the host's request, the Power-On procedure has succeeded and further tests can be carried out by proceeding to the uppermost level of the fault finding tree.

If no acknowledge is received, then proceed to 1.7.1

1.7.1 RS-Buffer Activated?

If the service software cannot receive the acknowledgement, then the fault can be in the CPU (D130), in the boot code that is located in the UCS Flash device (D163), or in the connection between the CPU and the host PC.

First check the connection:

During startup the CPU (D130) enables the RS-buffer MAX3222 (D180) by setting the RSENX (D180/pin1) low, RSSHDX (D180/pin20) high and the IRSHD (M180/pin6) high. The signals RSENX and the RSSHDX are toggled for the period of time that the CPU waits for a ping from the host, typically 3.5s. Check if this happens and whether the signal levels are OK.

If the signals are OK, then proceed to 1.7.2. If the CPU does not control the lines correctly, then proceed to 1.7.1.1

1.7.1.1 Valid Boot Code in UCS Flash?

If the boot code in the D163 is corrupted, then proceed to the 1.1. If the Flash is programmed, or it is sure that it contains valid data, and the CPU doesn't control the RS-buffer correctly, then proceed to 1.7.1.3

1.7.1.2 Program UCS Flash

If there's no guarantee that the UCS Flash (D163) contains a valid boot code, re-programme it with the JTAG method, or change to a good one. After programming / replacing, return to 1.6

1.7.1.3 CPU, or UCS-Flash Fault

If the CPU (D130) doesn't control the RS-buffer although there is a valid boot code in the UCS Flash (D163), then there is a fault either in the CPU, or in the Flash itself. In most cases the fault is likely to be the CPU, but it cannot be guaranteed unless the functionality of the UCS Flash is verified with another system.

1.7.2 Activity in CPU RxD0 ?

If the RS-buffer is activated and the IR-tranceiver TFDS3000 (M180) is put to active shutdown, then it's worth checking if the RSRXD line (D130/pin114 –D180/pin10) is toggling, i.e. are the host's pings received this far. If the line is toggling, and the signal levels are OK, then the CPU receives the ping bytes.

If the RSRXD line is not toggling, but the input of the buffer RXD (D180/pin9) is toggling, and the buffer control signals are OK, then proceed to 1.7.2.1. If the RSRXD signal is toggling (in the CPU pin), then the CPU should be transmitting acknowledgement bytes to the host. In the case proceed to 1.7.3

1.7.2.1 RS-Buffer Fault

In the case that the signals seem to stop to the buffer (D130), although the buffer control signals are set OK, then the buffer is likely to be defective.

1.7.3 Activity in CPU TxD0?

If the CPU receives the pings, then it should send acknowledgements through the RS-buffer to the service software. If the RSTXD line is not toggling, but the RSRXD is, then proceed to 1.7.1.1. If the RSTXD line is toggling but the TXD is not, then go to 1.7.2.1.

2 Troubleshooting Diagram of the POST-Code

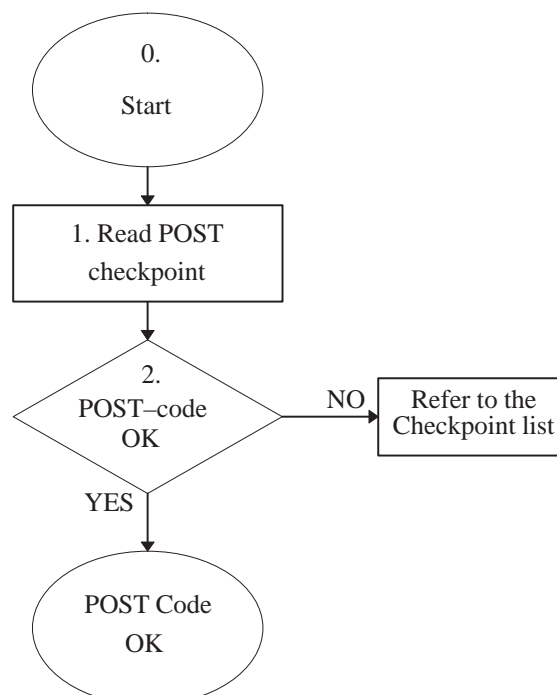
If the communications channel between the PDA and the service software can be established, the last checkpoint passed during POST can be retrieved from the PDA. The list of the POST-codes is in appendix B.

2.1 Read POST Checkpoint

In order to read the POST checkpoint, choose the Get POST Checkpoint menu in the PC Locals.

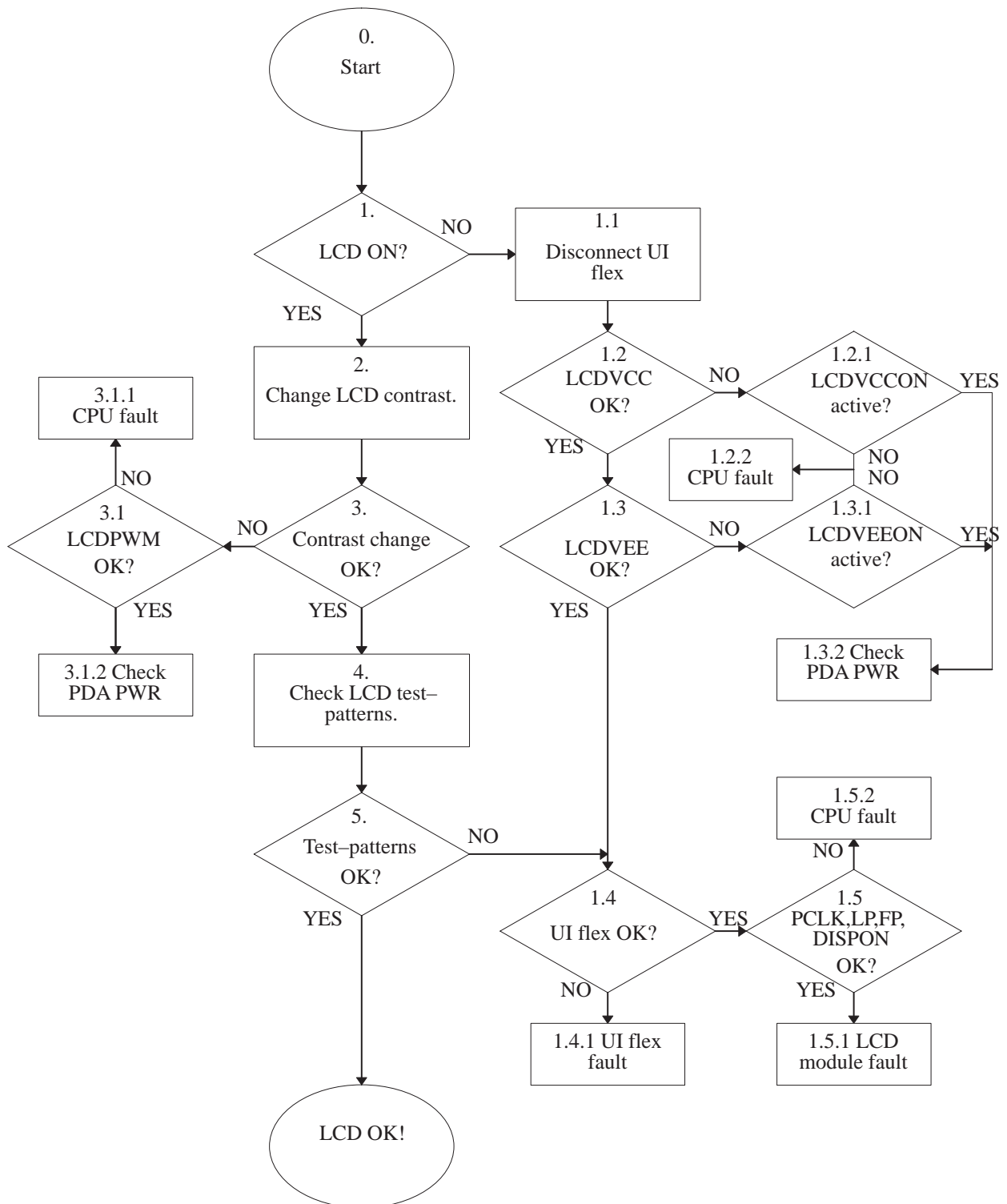
2.2 POST-code OK?

If the checkpoint is right, i.e. equal to the one last in the list, the POST has completed successfully, and there are no bad errors in the internal parts of the CPU and none in the DRAM. If the checkpoint differs from the one that is expected, then refer to the checkpoint list. The possible errors can be divided mainly into two groups; CPU-, and DRAM-related errors.



3 Troubleshooting Diagram of the LCD Check

The following diagram is to differentiate between an LCD module or a PDA fault. An LCD module fault is beyond the scope of this document and requires that a replacement module be fitted.



3.1 LCD ON?

The first step is to check whether the LCD is on when in testmode. When the PDA boots, and if the testmode pin is active, the CPU controls the LCD on. If the LCD remains blank, then proceed to 3.1.1. If the LCD is set on, then more detailed tests can be carried out when proceeding to 3.2

3.1.1 Disconnect UI Flex

In order to isolate the problems in the LCD module, disconnect the UI flex from the PDA. Of course it can be easily tested if the problem disappears when connecting a working LCD module to the PDA.

If the problem can be isolated to the PDA module, then proceed to 3.1.2

3.1.2 LCDVCC OK

Check if the LCDVCC is within its legal limits 4.5V..4.8V. If not, then proceed to 3.1.2.1. If yes, then go to 3.1.3

3.1.2.1 LCDVCCON active

If the LCDVCCON is active (high) but the LCDVCC level is out of the limits then proceed to 3.1.3.2. If the CPU does not control the LCDVCCON active, then go to 3.1.2.2

3.1.2.2 CPU Fault

If the CPU does not control either the LCDVCCON or / and the LCDVEEON, and the signals are not forced low in the PDA power unit, then the CPU is defective.

3.1.3 LCDVEE OK?

Check if the LCDVEE is within its legal limits 19V..23V. If not, then proceed to 3.1.3.1. If yes, then go to 3.1.4

3.1.3.1 LCDVEEON Active?

If the LCDVEEON is active (high) but the LCDVEE level is out of the limits then proceed to 3.1.3.2. If the CPU does not control the LCDVCCON active, then go to 3.1.2.2

3.1.3.2 Check PDA Power Unit

If the CPU controls the LCDVCCON active, but the LCDVCC is out of the limits, check the PDA power unit. Check components V80, V86, R81, R72 and C91.

In a case that the CPU controls the LCDVEEON active, but the LCDVEE is out of the limits, check the PDA power unit. If voltage at positive terminal of C89 is not between 20V and 24V go to PDA power unit complete check to 3.1.1. Check V84, R75, R76 and R96. There must be 4.1V voltage difference over V84. If OK check that N83 pin 4 is in low

logic level voltage (0 – 0.3V). If not replace N82.
Otherwise check V87 and V82. Voltage at gate pin of V82 should be one third of the voltage seen at plus terminal of C89. Voltages at LCDVEE line and C89 plus terminal must be practically equal.

3.1.4 Check UI Flex

In a case that the LCDVCC and the LCDVEE are within their voltage limits, the fault is likely in the other controlling signals. But first it is good to check the UI flex. If the UI flex is OK, proceed to 3.1.5, otherwise go to 3.1.4.1

3.1.4.1 UI Flex Fault

Change the UI Flex.

3.1.5 Check PCLK, LP, FP, DISPON

If the CPU does control the PCLK, LP, FP and the DISPON in a reasonable manner, then proceed to 3.1.5.1. If one of the synchronizing signals (PCLK, LP, FP) remain still all the time, or if the DISPON is inactive (low), then go to 3.1.5.2

3.1.5.1 LCD Module Fault

If all the control signals are OK at the end of UI flex, then the possible fault is either in the LCD module or in the UI module.

3.1.5.2 CPU Fault

If the CPU does not control all the signals as it should it is likely to be defective.

3.2 Change LCD Contrast

To check the functionality of the contrast controlling circuitry, choose the LCD test from the service software. Choose any test picture and then the desired contrast value 0..255, where 0 is the darkest and the 255 the lightest.

3.3 Contrast Change OK?

Test if the contrast changing works at least with two different contrast values. If the contrast seems to be good in the middle, low and high of the tunable range, then proceed to 3.4. If the contrast does not change, or if the range bad, then proceed to 3.3.1

3.3.1 LCDPWM OK?

Test if the duty factor of the PWM output of the CPU (D130/pin134) is changing according to the value given in the LCD test with the service software. If the level of the LCDPWM is OK, and the duty factor is changing from 1/255 to 254/255 then proceed to 3.3.1.2, otherwise go to 3.3.1.1

3.3.1.1 CPU Fault

If the CPU does control the PWMOUT signal correctly, even though the signal is disconnected from the PDA power unit, then it is likely that the CPU is at fault.

3.3.1.2 Check PDA Power Unit

The LCDV_{EE} output of the PDA power unit should change within the legal limits according to the PWMOUT signal duty factor. If the PWMOUT signal is controlled OK, but the LCDV_{EE} voltage doesn't change, then check the PDA power unit. Check components R86, C90 and R83.

3.4 Check LCD Test-Patterns

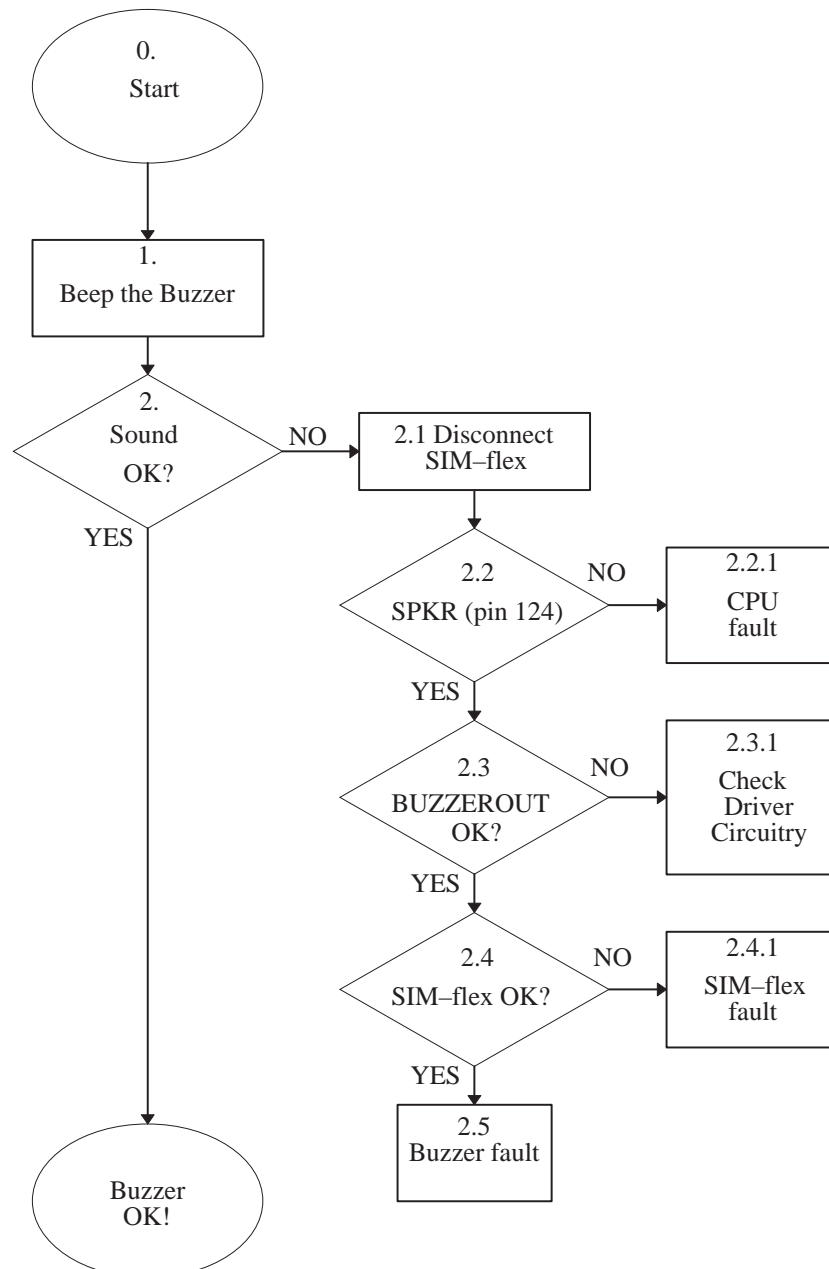
In order to check the functionality of every pixel on the LCD, various test patterns can be produced by selecting the LCD test in the service software.

3.5 Test-Patterns OK?

If all the pixels on the LCD toggle, the LCD test can be considered to have been successful. If there are some pixels / patterns that are not OK, then return to 3.1.4

4 Troubleshooting Diagram of the Buzzer

The functionality of the buzzer can be checked with the Service Software. The buzzer test tests the timer controls along with some other internal functions of the CPU.



4.1 Beep the Buzzer

To beep the buzzer, choose the buzzer test in the service software. Give the desired frequency and the duration.

4.2 Sound OK?

Listen to the sound, or optionally measure the output of the BUZZEROUT with an oscilloscope. If the frequency and the level are correct, then proceed to 4.2.1 otherwise the buzzer can be considered to be functional.

4.2.1 Disconnect SIM-Flex

In order to isolate the fault to the PDA module, disconnect the SIM-flex.

4.2.2 SPKR (pin 124)

Check the output of the pin 124 in the CPU (D130). Output should be a square wave at a given frequency. If the signal is not toggling, go to 4.2.2.1 If the CPU controls the output ok, then proceed to 4.2.3

4.2.2.1 CPU Fault

If the CPU does not control the SPKR output, even though the buzzer test is reported to be successful by the service software, then the CPU is likely to be faulty.

4.2.3 BUZZEROUT OK?

If the BUZZEROUT is OK then proceed to 4.2.4, otherwise the fault is in the buzzer driver circuitry; proceed to 4.2.3.1

4.2.3.1 Check Driver Circuitry

If the SPKR output stops before BUZZEROUT, check the circuitry R142-R148, V132-V135, C138.

4.2.4 SIM-Flex OK?

Check if the SIM-flex, and all the connectors are OK. If the connection from BUZZEROUT to the buzzer is OK, then proceed to the 4.2.5, otherwise go to 4.2.4.1

4.2.4.1 SIM-Flex Fault

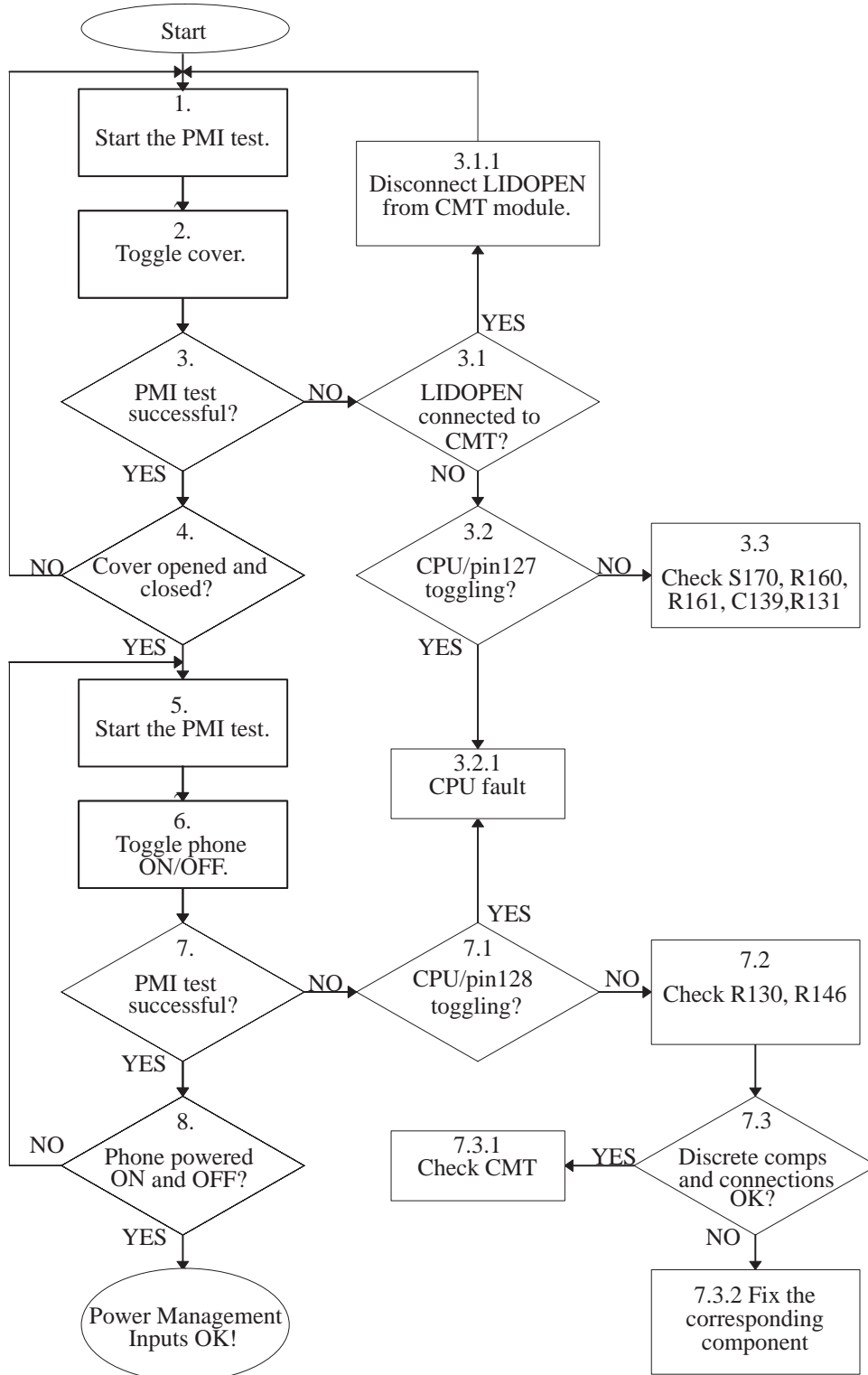
If the connection between the BUZZEROUT and the buzzer is broken, check the SIM-flex along with the board-to-board connectors, CMT module etc.

4.2.5 Buzzer Fault

If the CPU driven square wave is coming to the buzzer, but the buzzer does not beep, then change the buzzer.

5 Troubleshooting Diagram of the PMI Check

Once this test is activated the PDA waits for a power management interrupt to occur. The two possible sources for this interrupt are the lid-switch and the power switch of the CMT module.



5.1 Start the PMI Test

Start the PMI test by choosing the PMI test in the service software. Give a reasonable timeout value within which the interrupt is likely to occur.

5.2 Toggle Cover

In order to generate an interrupt, toggle the cover open or close.

5.3 PMI Test Successful?

If the service software reports the PMI test to been successful, proceed to 5.4 otherwise go to 5.3.1

5.3.1 LIDOPEN Connected to CMT?

In order to isolate the fault to the PDA module check if the LIDOPEN signal is connected to the CMT module. If the signal is connected go to 5.3.1.1 otherwise continue to 5.3.2

5.3.1.1 Disconnect LIDOPEN from the CMT Module

In order to isolate the fault to the PDA module, disconnect the CMT module. Proceed back to 7.1.

5.3.2 CPU pin 127 Toggling?

Check if the CPU pin 127 toggles according to the lid switch. The toggling can be checked by moving a magnet on the S170, or just by short circuiting it. If the pin does not toggle, then proceed to 5.3.3 otherwise go to 5.3.2.1

5.3.2.1 CPU Fault

If the CPU pin 127 (PMI0) or pin 128 (PMI1) is toggling while the PMI test is armed, and the PCLocals reports the test to have been unsuccessful, then it is likely that the CPU is not working correctly.

5.3.3 Check S170, R149, R150, R151, C139

If the signal is not toggling, change the faulty component.

5.4 Cover Opened and Closed?

Repeat the test switching the cover to the opposite position, i.e opened → close and closed → open. Goto 5.5

5.5 Start the PMI Test

Start the PMI test by choosing the PMI test in the service software. Give a reasonable time-out value within which the interrupt is likely to occur.

5.6 Toggle Phone ON/OFF

In order to generate an interrupt, toggle the CMT module ON or OFF.

NOTE: *the CMT switches OFF several seconds after the power switch has been pressed!*

5.7 PMI Test Successful?

If the service software reports the PMI test to been successful, proceed to 5.8 otherwise go to 5.7.1

5.7.1 CPU pin 128 Toggling?

Check if the CPU pin 128 toggles according to the power ON/OFF switch of the CMT. If the pin does not toggle, then proceed to 5.7.2 otherwise go to 5.3.2.1

5.7.2 Check R130, R146

If the signal is not toggling, check the resistors.

5.7.3 Discrete Components and the Connections OK?

If the resistors and the connections to the CMT module are OK, proceed to 5.7.3.1 otherwise go to 5.7.3.2

5.7.3.1 Check CMT

If the resistors and the connections to the CMT module are OK, then the fault is in the CMT module.

5.7.3.2 Change the Corresponding Component

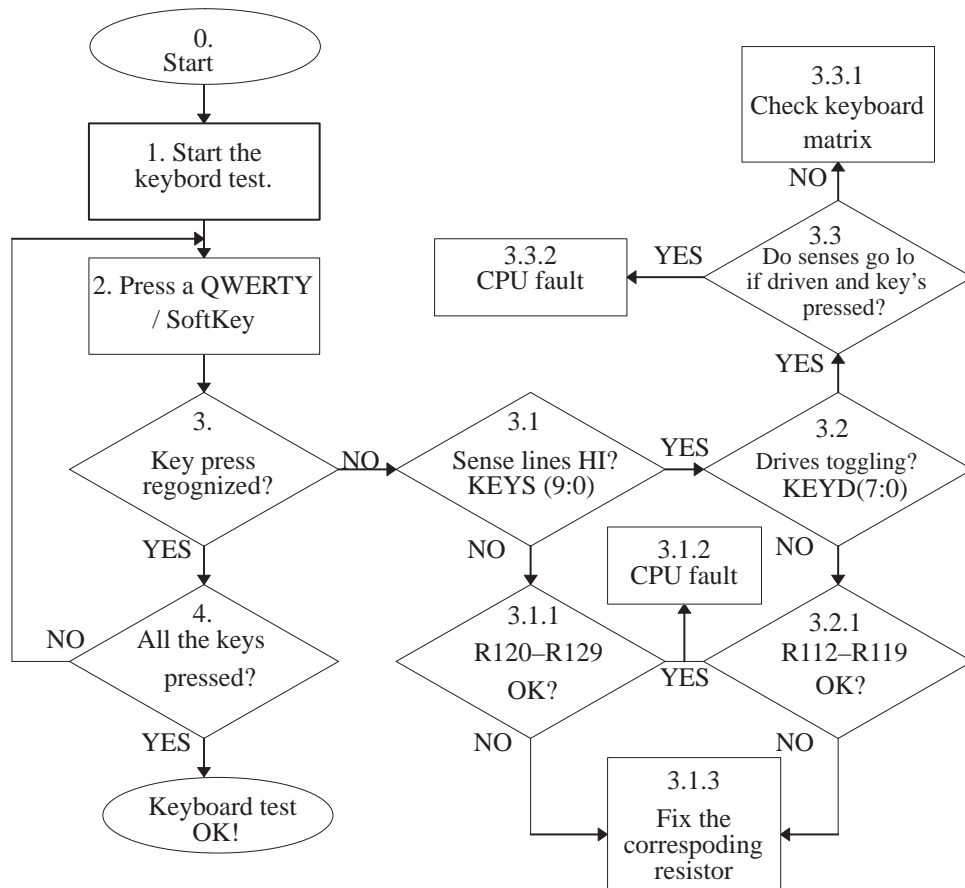
Change the bad resistor.

5.8 Phone Powered ON and OFF?

Do the test using both transitions phone OFF → switch the phone ON, phone ON → switch the phone OFF. If both transitions were successful, the PMI test can be considered to have been successful.

6 Troubleshooting Diagram of the Keyboard

The following picture illustrates the troubleshooting diagram of the keyboard. Once the keyboard test is started, all the keys of the PDA can be tested.



6.1 Start the Keyboard Test

Start the keyboard test with the service software. The test waits for a key-press within the given time period.

6.2 Press a QWERTY / Softkey

Press a key on the QWERTY keyboard or one of the soft-keys of the PDA.

6.3 Key Press Recognized?

If the key was recognized it prints the name of the key on the screen. If a legal combination of keys are pressed simultaneously, all the pressed keys are shown on the screen. If the key-press was not recognized then proceed to 6.3.1 otherwise go to 6.4

6.3.1 Sense Lines HI, KEYS (9:0)?

Pressing a key draws the sense line low, from idle high state, where it is connected in the keyboard matrix. Therefore, if no key is pressed, all the KEYS sense lines should be in a logic high state. Should this happen, continue to 6.3.2 otherwise proceed to 6.3.1.1

6.3.1.1 R120-R129 OK?

Check the sense line pull-ups. If the resistors are OK, then proceed to 6.3.1.2 otherwise go to 6.3.1.3

6.3.1.2 CPU fault

If the pull-ups R120-R129 are OK, then it is likely that the CPU (D130) is pulling the sense-line low. Expect a CPU fault.

6.3.1.3 Fix the Corresponding Resistor

Change the faulty resistor.

6.3.2 Drives Toggling KEYD(7:0)?

Once the keyboard test is running, it drives the keyboard drive lines from idle high to low state one by one, one at a time. If one or more line(s) remain fixed low or high, go to 6.3.2.1

6.3.2.1 R112-R119 OK?

The keyboard matrix is driven through the series resistors R112-R119. Check if all the resistors are OK. If the resistors are OK, go to 6.3.1.2 if not go to 6.3.1.3

NOTE: Resistors R112-R119 are installed only in CPU versions A3 or A5. If A7 version of the CPU is used, the resistors are not installed. Also if the A7 version of the CPU is used, then the value of the resistors R120-R129 is changed!

6.3.3 Do Senses Go Low if Driven and a Key Is Pressed?

Press a key in the matrix and scope the corresponding sense line. If the drive line is driven, but the sense line remains high proceed to 6.3.3.1 otherwise go to 6.3.3.2

6.3.3.1 Check keyboard matrix

If the sense line remains high, even though it should be forced low when driven, expect a fault on the circuit connections. Although the CPU can force the senses high also.

6.3.3.2 CPU Fault

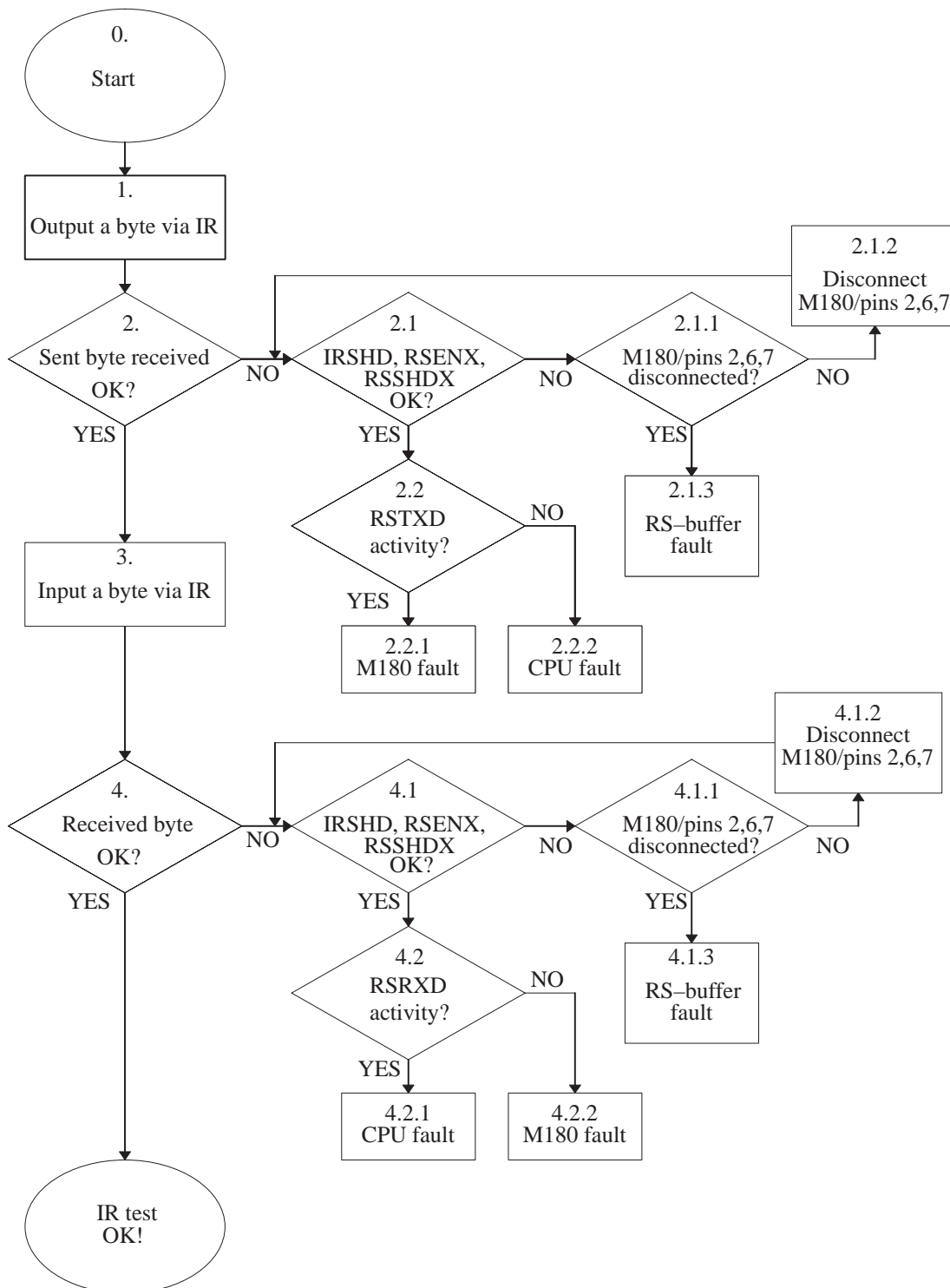
If the sense lines toggle according to the pressed keys on the keyboard when they are driven, then the CPU is likely to be defective.

6.4 All the Keys Pressed?

If all the keys are pressed, and they have been recognized correctly, the keyboard test can be considered to have been successful. If all the keys have not been tested, go back to 6.2

7 Troubleshooting Diagram of the InfraRed Check

The following picture illustrates the troubleshooting diagram of the infrared test. Only half duplex method is supported for testing the IR connection.



7.1 Output a Byte via IR

Start the IR test from the service software. Select output mode and the byte to send from the 9000. The external IR tranceiver should be connected to the other serial port, where the DLR-1 cable is connected.

7.2 Sent Byte Received OK?

If the service software can receive the byte sent, continue to 7.3 otherwise proceed to 7.2.1

7.2.1 IRSHD, RSENX, RSSHDX OK?

When the byte is sent, it toggles the RSENX from logic low to high, RSSHDX at the same time from logic high to low, and after few milliseconds the IRSHD from logic high to low. If these signals do not toggle correctly, proceed to 7.2.1.1 If the signals are OK, then go to 7.2.2

7.2.1.1 M180 / pins 2,6,7 Disconnected?

To isolate a problem with the IRSHD, RSENX and the RSSHDX that does not control the RS-buffer and the M180 IR tranceiver module correctly, disconnect the control signals from the M180. If the pins are connected continue to 7.2.1.2, otherwise go to 7.2.1.3

7.2.1.2 Disconnect M180 / pins 2,6,7

By doing this, the control signals can be isolated to the RS-buffer or to the CPU. Go back to 7.2.1

7.2.1.3 RS-Buffer Fault

If the control signals do not toggle to the right state, even though the IR tranceiver is isolated, then the fault is most likely in the RS-buffer (D180). However it is possible, that the CPU does not control the lines. But since the RS-buffer is needed for the communications to the host, it can not be tested, if the control signals are disconnected between the CPU – RS-buffer.

7.2.2 RSTXD Activity?

If the byte is already sent to the IR tranceiver, then the RSTXD line toggles immediately after the control signals are toggled. If the RSTXD signal toggles proceed to 7.2.2.1 otherwise go to 7.2.2.2

7.2.2.1 M180 Fault

If all the signal lines to the IR tranceiver toggle as they should, the M180 is likely to be faulty.

7.2.2.2 CPU Fault

If the RSTXD signal does not toggle, then the CPU is likely to be faulty.

7.3 Input a Byte via IR

If the sending of a byte was successful, try then to receive one. Choose the Input mode in the service software, and choose a byte to be received.

7.4 Received Byte OK?

If the service software reports success, the IR test can be considered to have been successful, otherwise proceed to 7.4.1

7.4.1 IRSHD, RSENX, RSSHDX OK?

When the 9000 begins to receive the byte, it toggles the RSENX from logic low to high, RSSHDX at the same time from logic high to low, and after few milliseconds the IRSHD from logic high to low. If these signals do not toggle correctly, proceed to 7.4.1.1. If the signals are OK, then go to 7.4.2

7.4.1.1 M180 / pins 2,6,7 Disconnected?

To isolate a problem with the IRSHD, RSENX and the RSSHDX that does not control the RS-buffer and the M180 IR tranceiver module correctly, disconnect the control signals from the M180. If the pins are connected continue to 7.4.1.2, otherwise go to 7.4.1.3

7.4.1.2 Disconnect M180 / pins 2,6,7

By doing this, the control signals can be isolated to the RS-buffer or to the CPU. Go back to 7.4.1

7.4.1.3 RS-Buffer Fault

If the control signals do not toggle to the right state, even though the IR tranceiver is isolated, then the fault is most likely in the RS-buffer (D180). However it is possible, that the CPU does not control the lines. But since the RS-buffer is needed for the communications to the host, it can not be tested, if the control signals are disconnected between the CPU – RS-buffer.

7.4.2 RSRXD Activity?

If the byte is received by the IR tranceiver, then the RSRXD line toggles right after the control signals are toggled. If the RSRXD signal toggles proceed to 7.4.2.1, otherwise go to 7.4.2.2.

7.4.2.1 CPU Fault

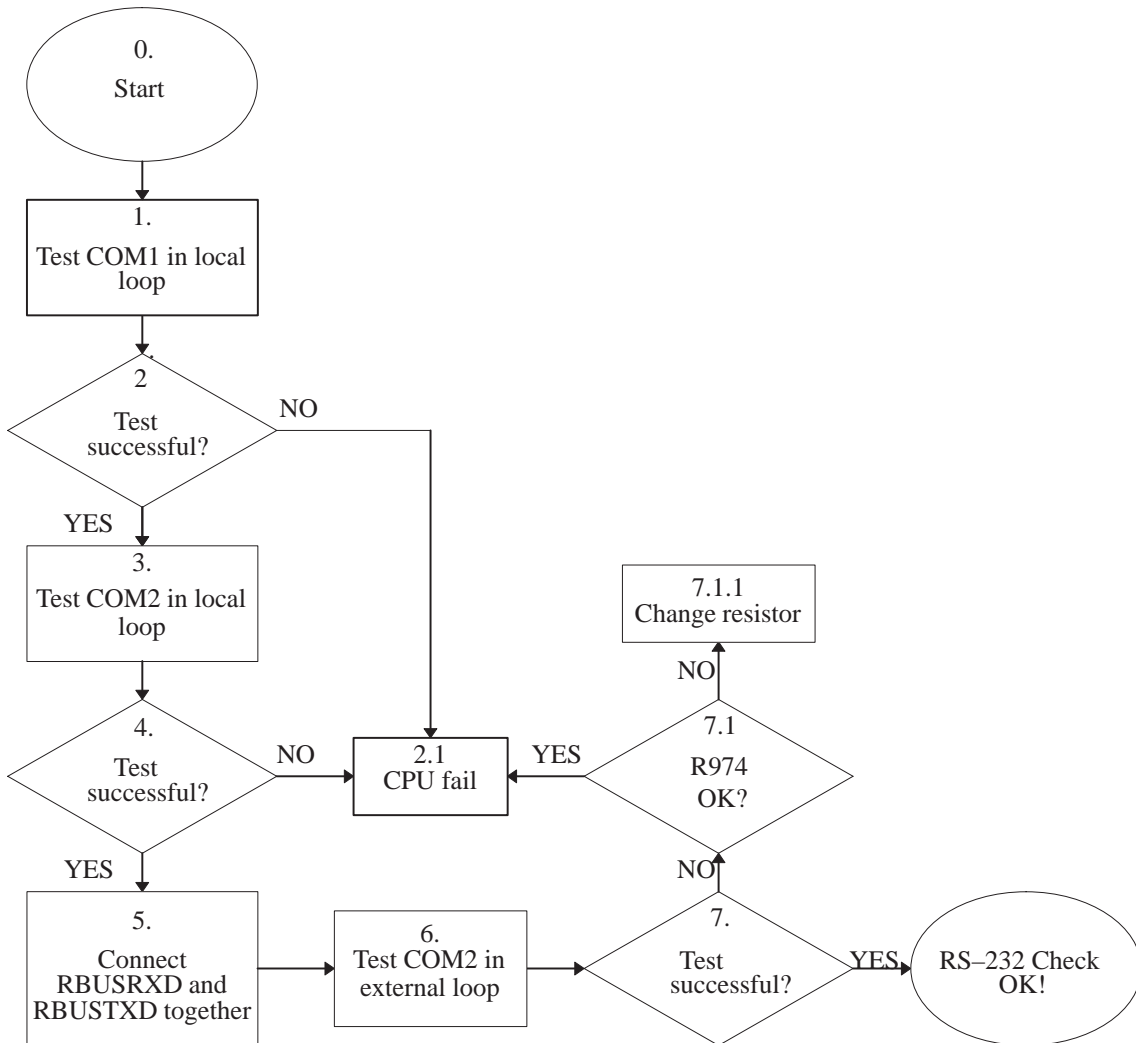
If all the signal lines to the IR tranceiver toggle as they should, and there is activity in the RSRXD while the IR transmitter connected to the host PC is transmitting the byte, then the CPU is likely to be faulty.

7.4.2.2 M180 Fault

If the RSRXD signal does not toggle, then the M180 is likely to be faulty.

8 Troubleshooting Diagram of the RS-232 Check

The following picture illustrates the serial port tests. As the COM1 is being tested automatically in the communications to the host PC, only the COM2 can be tested externally with the aid of the service software. Both serial ports can be tested in the UART's local loop.



8.1 Test COM1 in Local Loop

Choose the serial test in the service software and select COM1 to be tested in a local loop. The test is ran at the same baud rate that is used in the communications to the host PC.

8.2 Test Successful?

If the test passes successfully proceed to 8.3, otherwise branch to 8.2.1

8.2.1 CPU Fault

If either of the tests in the local loop mode fails, then the CPU is defective.

8.3 Test COM2 in Local Loop

Select the COM2 to be tested in the local loop. The test is ran at 9600 baud by default.

8.4 Test Successful?

If the test passes successfully proceed to 8.5, otherwise branch to 8.2.1

8.5 Connect RBUSRXD and RBUSTXD Together

In order to test the external lines of the COM2, the RBUSRXD and RBUSTXD may be connected together e.g. in the board-to-board connector. When testing the COM2 in this external loop, the bytes are received via this connection.

8.6 Test COM2 in External Loop

Choose in the service software the COM2 test in external loop.

8.7 Test Successful?

If the test passes in the external loop, the serial ports can be considered to be functional, otherwise continue to 8.7.1

8.7.1 R947 OK?

There is only one resistor between the CPU pins 97-98, check it along with the connections. If OK, go to 8.2.1, if not go to 8.7.1.1.

8.7.1.1 Change Resistor

Change the faulty R974.

Appendix A

POST beep codes, number of beeps:

- | | |
|----|---|
| 1 | Memory refresh is not working. |
| 3 | Memory failure in 1st 64KB of memory. |
| 4 | Timer T1 not operational. |
| 5 | CPU test failed. |
| 6 | Gate A20 failure. |
| 10 | CMOS shutdown register failed. |
| 13 | Exhaustive low memory test failed. |
| 14 | Exhaustive extended memory test failed. |
| 15 | CMOS restart byte can't hold data. |
| 16 | Address line test failed. |
| 18 | Interrupt controller failure. |

Appendix B

POST progress codes. These are written during POST to the IO address 2FFh, and if the BIOS-testmode is entered the last code is copied to the IO address 3FFh.

00h	POST beginning
01h	CPU register test starting
05h	Disabling shadowing & cache
0Dh	Test CMOS RAM shutdown register
0Eh	Check CMOS checksum, update DIAG byte
11h	Disable interrupts controllers
12h	Disable Port B and video display
13h	Initialize chipset and start auto memory detect
15h	Test 8254 Timer2 for speaker, Port B
16h	Test 8254 Timer1 for refresh
17h	Test 8254 Timer0 for 18.2Hz
18h	Start memory refresh
1Ah	Test 15 us refresh ON/OFF time
19h	Test memory refresh
20h	Test address lines
22h	Base 64kB memory read/write test
23h	System initialization before vector table init
24h	Initialize vector table
35h	Check ROM BIOS data area at segment 40h
40h	Prepare virtual memory test, verify from display memory
42h	Enter virtual mode for memory test
44h	Initialize data for checking wraparound at 0:0
4Ch	Clear extended memory for soft reset
4Dh	Save memory size
53h	Save registers & memory size, enter real-mode
55h	Disable A20 line
66h	Initialize interrupt controllers
82h	Initialize circular buffer
84h	Check for memory size mismatch (CMOS/BIOSDATA)
8Fh	Configure floppy drives
94h	Set base & extended memory sizes
95h	Memory size adjusted for 1k, verify display memory
96h	Initialization before calling C800h
97h	Call ROM BIOS extensions at C800h
98h	Processing after extension returns
99h	Configure timer data area
A6h	Enable NMIs

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